RERAM COMPUTE CROSSBAR FABRICATION

DESIGN DOCUMENT I

Authored by

Konnor Kivimagi, Jason Xie, Gage Moorman, and Nathan Cook

Advised by

Dr. Henry Duwe and Dr. Cheng Wang

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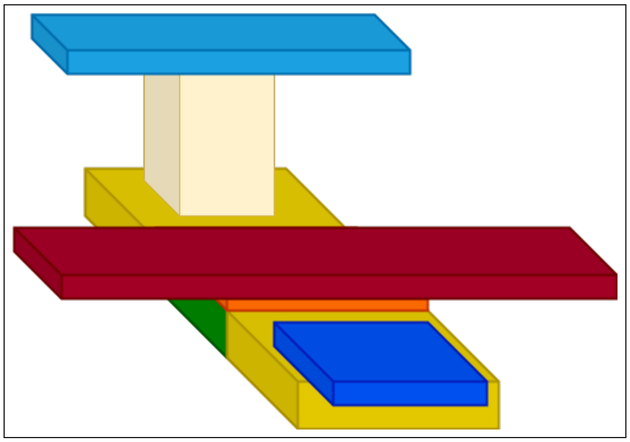

Team contact: sddec24-13@iastate.edu
Team website: https://sddec24-13.sd.ece.iastate.edu/

Executive Summary

Development Standards and Practices Used

- IEEE 1076.4-2000 - IEEE Standard VITAL ASIC Modeling Specification
  - Promotes the development of highly accurate, efficient simulation models for ASIC (Application Specific Integrated Circuit) components in VHDL.
- IEEE 1481-2019 - IEEE Standard for Integrated Circuit (IC) Open Library Architecture(OLA)
  - Methods to analyze chip timing and power consistently across a broad set of electric design automation (EDA) applications
- IEEE 1149.4-2010 - IEEE Standard for a Mixed-Signal Test Bus
  - Defines a mixed-signal test bus architecture that provides the means of control and access to both analog and digital test signals
- IEEE 1364-2005 - IEEE Standard for Verilog Hardware Description Language
  - Defines verilog hardware description language

Summary of Requirements

- Functional requirements
  - Low overall power consumption
  - Ensure the DAC outputs correct voltage thresholds
  - ADC will have a higher than 1-bit resolution (3-4 bits)
  - Low-power trans-impedance amplifier
- UI requirements
  - The ability to see what is happening on the inside for conducting research
  - Require IO ports for probe testing

Applicable Coursework from Iowa State University

- EE230 - Electronic Circuits and Systems
- EE330 - Integrated Electronics
- EE435 - Analog VLSI Circuit Design
- EE465 - Digital VLSI Circuit Design
- CprE 281 - Digital Logic

New Skills/Knowledge Acquired

- ReRAM technology
- Open-source design using Xschem, Magic VLSI, and Ngspice
- Skywater 130nm process
- ASIC design

Contents

List of Tables

List of Figures

1 Introduction

1.1 Problem Statement

Resistive random access memory(ReRAM or RRAM) is an emerging, non-volatile, low-power memory technology. ReRAM has a significant appeal due to its scalability at smaller processes and a much higher capability for memory density.

This project aims to create a research vehicle for silicon, proving computational resistive random access memory(ReRAM or RRAM) for research and education purposes. ReRAM allows for computation within the memory, eliminating the need to send data to and from a digital ALU(Arithmetic logic unit).

The current issues this project faces are a need for produced ReRAM chips, limited opportunities to get chips fabricated, and a test vehicle to gain an understanding of and better test the physical characteristics of ReRAM primitives in Skywater technology.

ReRAM technology is primarily used as a memory device. Therefore, understanding how it interacts with peripheral circuits while being implemented for computation is essential for our project and will be one of the goals of this project. Due to ReRAM being an emerging technology, there are multiple questions that we would like to answer. One major question is whether or not using ReRAM for computation is better than existing memory technologies. A few ways to measure this could be to compare computation accuracy, energy efficiency, and power consumption between ReRAM and a similar technology such as SRAM or DRAM.

1.2 Users and User Needs

Professor Duwe and Professor Wang:

The primary intended users for this project are Prof. Duwe and Prof. Wang. They are also the clients of this particular project. The results of our project would provide them with a practical example of a ReRAM compute crossbar and knowledge of how the Efabless process can be used to design and fabricate chips in the Skywater 130nm process.

Graduate students:

These students would most likely be the graduate students that are under Prof. Duwe and Prof. Wang. These students would need documentation on the Efabless process and tool flow to apply that knowledge to their projects. This documentation would benefit them by understanding the process they are to use and allowing them to focus solely on their design.

Undergrad students:

These students will be able to bring up our chip and others fabricated under Duwe as a part of their undergraduate curriculum. These students will need easy-to-follow lab documentation similar to EE 201 and 230. The benefit these students receive is the ability to bring up and test a physical chip in parallel with their regular course work, providing them valuable experience and real-world experience of the concepts they are learning.

2 Requirements, Constraints, and Standards

2.1 Requirements and Constraints

- Functional requirements:
  1. Low overall power consumption
  2. Ensure the DAC outputs correct voltage thresholds
  3. ADC will have a higher than 1-bit resolution
  4. Low-power trans-impedance amplifier
- Deliverables:
  1. Git repo with all project files
  2. Project documentation
     - Bring up documentation
     - Lab walkthrough documents
     - Probe testing documentation
     - Top-level circuit diagram
  3. Simulations showing correct device operations
- User requirements:
  1. Bring up documentation for success/failure
- Precheck approved GS2:
  - All subcircuits need to pass Design Rule Check(DRC) and Layout Versus Schematic (LVS)
  - The final design must be integrated with Caravel Harness and Pass LVS
- UI requirements:
  - The ability to see what is happening on the inside for conducting research
  - Require IO ports for probe testing

2.2 Engineering Standards

- IEEE 1076.4-2000 - IEEE Standard VITAL ASIC Modeling Specification
  - Promotes the development of highly accurate, efficient simulation models for ASIC (Application-Specific Integrated Circuit) components in VHDL.
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3 Project Plan

3.1 Project Management/Tracking Procedure

The project management style that we will use is AGILE. This methodology was chosen due to its iterative nature, allowing us to constantly check and verify that we have completed our goals before we continue to the next step. We will track progress through Microsoft Teams.

3.2 Task Decomposition

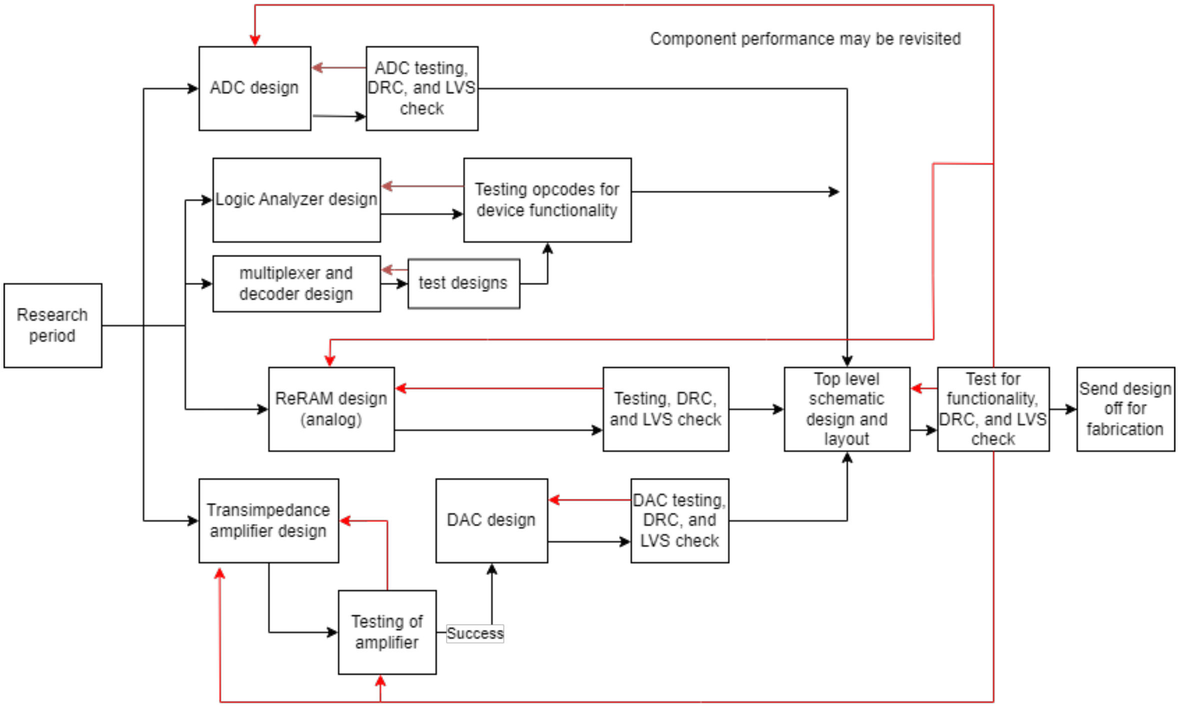

Component performance may be revisited
ADC design
ADC testing, DRC, and LVS check
Logic Analyzer design
Testing opcodes for device functionality
multiplexer and decoder design
test designs
Research period
ReRAM design (analog)
Testing, DRC, and LVS check
Top level schematic design and layout
Test for functionality, DRC, and LVS check
Send design off for fabrication
Transimpedance amplifier design
DAC design
DAC testing, DRC, and LVS check
Testing of amplifier
Success

Figure 1: Task decomposition

Analog design will be split between Gage, Jason, and Konnor. Jason and Nathan will work on digital design. Everyone will work on the documentation.

3.3 Project Proposed Milestones, Metrics, and Evaluation Criteria

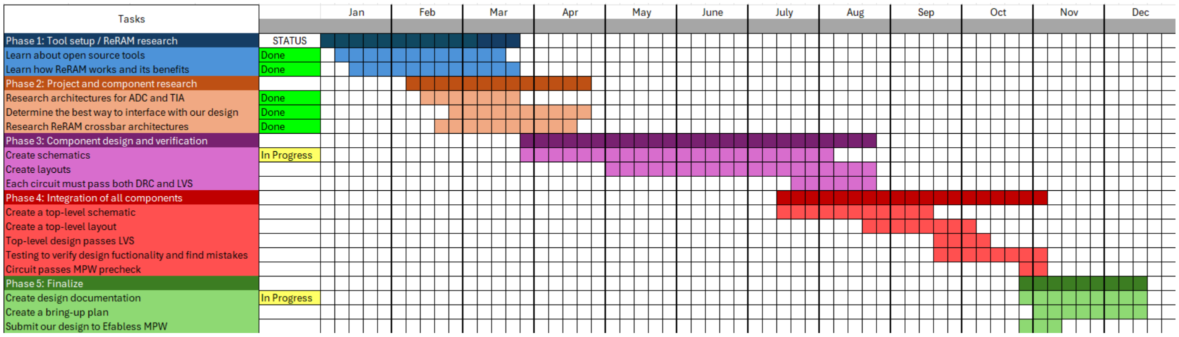
- Phase 1: Analog Tool Setup / ReRAM research
  - Verify that we can run all the tools needed for this project
- Phase 2: Project and component research
  - research applicable ADC, DAC, and TIA architectures
  - Develop a better understanding of ReRAM architectures
  - Determine the best interface methodologies and devices
- Phase 3: Component design and verification
  - All components must pass both LVS and DRC checks to be verified

    - Schematics created in Xschem, layouts created in Magic VLSI

- Phase 4: Integration of all components
    - Integrate all components into one top-level design and create a schematic and layout for this design
    - The schematic and layout must pass LVS
    - Simulate the system rigorously to verify that the integrated design is operating as expected

- Phase 5: Finalise documentation
    - Create design documents
    - Create a bring-up plan for the ReRAM

3.4 Project Timeline/Schedule



Tasks	
Phase 1: Tool setup / ReRAM research	STATUS
Learn about open source tools	Done
Learn how ReRAM works and its benefits	Done
Phase 2: Project and component research	
Research architectures for ADC and TIA	Done
Determine the best way to interface with our design	Done
Research ReRAM crossbar architectures	Done
Phase 3: Component design and verification	
Create schematics	In Progress
Create layouts	
Each circuit must pass both DRC and LVS	
Phase 4: Integration of all components	
Create a top-level schematic	
Create a top-level layout	
Top-level design passes LVS	
Testing to verify design fuctionality and find mistakes	
Circuit passes MPW precheck	
Phase 5: Finalize	
Create design documentation	In Progress
Create a bring-up plan	
Submit our design to Efabless MPW	

Figure 2: Project Timeline

3.5 Risks and Risk Management/Mitigation

In concerns of design and verification, peripheral circuits may not get done on time. We can mitigate this risk by planning well and designing circuits in other programs, such as cadence. We could also reduce the complexity of designs and reduce time to completion.

There is a risk concerning the digital functionality and performance of the memristor as the model provided by the PDK is currently inaccurate. It has been shown to simulate behavioral errors. Similarly, in the analog models of the CMOS transistors provided by the PDK, there is an inconsistency in simulation results during weak and moderate inversion conditions. A solution for both cases, albeit laborious and implausible considering the time constraints, we can attempt to resolve the model issues by either contributing to the open-source spice model or developing an entirely new model ourselves. A more likely solution would be to create sound documentation of the current issues of the model and derive plausible solutions for future teams.

When considering the fabrication process, there arises a risk in which the design constraints are not met due to fabrication errors. While preventing fabrication errors is beyond our sphere of influence, we can mitigate this risk by providing a sound bring-up plan with intricate specifications concerning testing methods and expected results.

3.6 Personnel Effort Requirements

Phase 1 Research and Setup		
Task	Time	Component
ReRAM and crossbar research	30 Hrs	Research the essential operation of ReRAM as well as how it is implemented as a crossbar for computation
Analog tool flow setup	20 Hrs	Setup of the essential tools we will need for design. These include Xschem, magic, and Ngspice
Consideration of how to design peripheral analog circuits	15 Hrs	Discuss the different structures and routes to take in our design process

Table 1: Phase 1: Research and Setup

Phase 2 and Phase 3 Component Design and Verification		
Task	Time	Component
Schematic creation	5 Hrs / Component	Create a schematic for each component in Xschem
Simulation and debugging of schematic	10 Hrs / Component	Run simulations with Ngspice on the schematics and make changes as necessary to achieve the desired functionality
Layout creation	10 Hrs / Component	Create a layout for the schematic in magic
Verification of component	10 Hrs / Component	Verify that the layout passes DRC and that the element passes LVS

Table 2: Phase 2 and 3: Component Design and Verification

Phase 4 Integration		
Task	Time	Component
Top-level schematic	25 Hrs	Implement a top-level schematic with all of the components
Top-level layout	30 Hrs	Implement the layout of the top-level schematic and verify that it passes LVS.

Table 3: Phase 4: Integration

System Verification		
Task	Time	Component
Top-level schematic	25 Hrs	Implement a top-level schematic with all of the components
Top-level layout	30 Hrs	Implement the layout of the top-level schematic and verify that it passes LVS.

Table 4: System Verification

Phase 5 Finalise		
Task	Time	Component
Create documentation	20 Hrs	Create documentation for our project detailing our process. As well as improving upon existing tools/software documentation
Create a detailed bring-up plan	35 Hrs	Document how our device should be tested to prove functionality and discover any discrepancies between simulations and testing of the fabricated chip

Table 5: Phase 5: Finalise

3.7 Other Resource Requirements

This project will be completed using open-source tools available to the general public; however, this results in poor documentation and resources available to us. Our most valuable resources are the open-source hardware slack channel and the documentation on the tools from previous teams.

4 Design

4.1 Design Context

Broader Context

ReRAM is a memory technology that has the potential to be able to perform computations in the analog domain. This can be beneficial as it minimizes data movement and, in turn, requires less power consumption than traditional digital computations. We aim to create a ReRAM crossbar to be fabricated through Efabless so that future students can bring up and test our design's functionality. Relevant considerations for multiple areas are listed in Table 6.

Area	Description	Examples
Public health, safety, and welfare	Our product does not have many direct impacts on public health, safety, and welfare. However, it is a possibility that a working implementation of our design could be helpful in many applications in the future	This technology brings with it the potential to create a new job market as breakthroughs in this could lead to a drive for companies each to have the best version of it
Global, cultural, and social	This is an open-source project so that we will adhere to the values of transparency, collaboration, and continual growth	This project will be fabricated through Efabless and must be submitted as a project to the open-source repository. This means that it could inspire others going forward
Environmental	The chip fabrication process is generally toxic. However, our design will only be fabricated once. ReRAM also has the potential to draw less power than its digital counterparts	Our project will implement a ReRAM crossbar that will hopefully allow for computations to be done in a more power-efficient way
Economic	Our project is being designed through open-source tools which are free to use	Our design will be added to the open-source documentation and will be free to view and use by anyone in the future

Table 6: Broader Context

Prior Work/Solutions

Not many existing references are available or able to be found commercially. The ReRAM is a developing technology, and many details are not readily available to the general public. However, we are using the open source forums through the company Efabless, where there has been some attempt at designing a ReRAM module. While it is not much, we have small stepping stones to go off of between this and the previous group's findings.

Technical Complexity

Our design is complex, consisting of both digital and analog components. These components include:

- Design of a ReRAM module:
    - Requires lots of research into how this memory technology works.
- Design of a Digital Logic Analyzer
    - Requires knowledge of Verilog and how to implement logic algorithms.
- Design of conversion circuits such as ADC and DAC
    - Must be designed for a specific resolution goal.
    - Requires design of encoders and decoders.
    - Requires knowledge of ADC architectures and which might best fit our project.
- Use of open-source tools
    - Requires reading documentation and troubleshooting setup issues.
    - These are much less polished than the tools used by large companies and, as such, are difficult to maneuver at times.
- Design of a TIA
    - Understanding the requirements for input and output ranges requirements and how to design around them.

4.2 Design Exploration

Design Decisions

In determining our project's aspects, we determined the peripheral circuitry based on the ReRAM operative parameters. Systemically, the peripheral circuitry serves as the interface between external accessibility and the operation of the ReRAM. At the highest description level, we first have the DAC (Digital to Analog Converters), which allows us to control the system through external digital excitation. Conversely, we also require an ADC (Analog to Digital Converter), which will enable us to realize the resulting analog output of the ReRAM. These well-studied circuits have plenty of references to allow us to design a system that satisfies our defined constraints.

However, once the ReRAM has processed the input, it returns a current that cannot be easily translated into a digital output, as existing ADC architectures are primarily designed to take voltage inputs. To remedy this, we will need a TIA (Transimpedance Amplifier) that converts a current into a voltage at a standard reference. Lastly, we also require miscellaneous circuitry that allows us to assume as much control over the ReRAM Crossbar as possible. We will use encoders and multiplexers to enable the ability to decipher and administer the previously mentioned external digital commands to the voltage controls on the ReRAM crossbar.

Overall, design decisions for each of these peripheral circuits will be based on the design constraints established by the project and parameter expectations from the desired ReRAM Crossbar architecture.

Ideation

As an example of our ideation process for the circuits, as mentioned above in section 4.1.1, we will cover the ADC. There are many pre-existing architectures we considered when designing our ADC. We started by referencing designs from a course textbook we were familiar with, leading us to discover the Flash, Pipelined, and SAR (Successive Approximation Converter) ADC.

The simplest of these, the Flash ADC, is a converter based on a parallel resistor and comparator string. Of the three architectures, the Flash ADC has the fastest conversion speed and is generally the easiest to implement. However, Flash ADC calls for an exponentially increasing amount of comparators to the number of bits. Not only does this aspect cause a more significant demand amount of area, but it also means the circuit becomes exponentially more power-hungry. Furthermore, due to the number of comparators on the input, there is a large number of parasitic capacitances, which could deter the speed of the ADC and require another power-hungry buffer to drive the input. An illustration of a general 3-bit flash ADC is shown in Figure 3. [1]

On the other hand, instead of a single conversion stage, the Pipelined ADC implements several circuits that algorithmically determine outputs via the simultaneous conversion of successive inputs. This is usually achieved through a series connection between an N/2-bit ADC and N/2-bit DAC, which results in an N-bit output resolution. If we use this system with a Flash ADC, we have effectively halved the area and power consumption in proportion to increasing the resolution while maintaining a relatively high throughput. Furthermore, because of the circuit's modularity and redundancy, multiple stages can be resolved in each stage, where any offset in the comparators can be rectified through digital correction. However, this digital correction cannot determine the nonlinearities in the DAC and inaccuracies in the interstage gain, which limits the overall performance of the ADC. Moreover, due to its algorithmic nature, Pipelined architectures typically require an input clock at the minimum, which also introduces latency issues. [1]

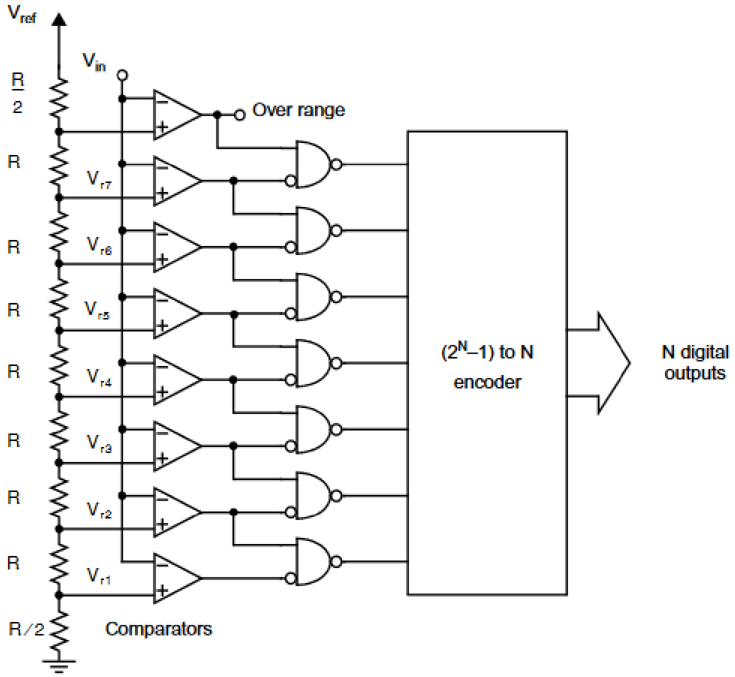


Figure 3: Example of Flash ADC circuit from [1]

Finally, the SAR ADC is another algorithmic-based converter that relies on some digital control logic to perform a binary search on a series input. The architecture, in general, can be relatively simplistic, containing a DAC, a digital control logic circuit, and a comparator. Furthermore, because the architecture is iterative and algorithmic, the SAR ADC scales linearly with resolution per the DAC specifications. This means much higher resolution and accuracy can be achieved with less power and space. Conversely, because of the iterative nature, this architecture has a relatively low throughput compared to the Flash and Pipelined ADC architectures. A general SAR ADC circuit is shown in Figure 4. 1]

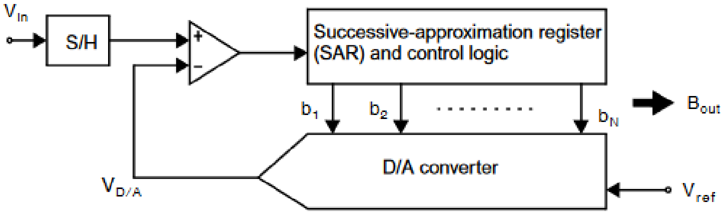


Figure 4: Example of SAR ADC circuit from [1]

Aside from the three architectures taken from our textbook, we also considered some ADCs used in research papers on ReRAM Crossbar. One example that stood out to us was the TDC (Time to Digital Converts). This architecture was proposed as time-domain data conversions are known to be more energy efficient compared to the traditional voltage to the digital domain. The conversion was done by establishing signal codes through the delay from an established point. This means the system can be implemented as a fully digital flow and remove the need for some peripheral circuits like the TIA entirely. Unfortunately, the typical TDC circuit is relatively complex and would require us to understand concepts beyond our curriculum and current experience.

Furthermore, implementing a TDC would require operating everything in a different domain. This would lead us to stray from the conventional control logic for the ReRAM crossbar and design and incorporate other peripheral circuits like a DTC (Digital to Time Converter). In other words, while the TDC is a compelling option to satisfy our constraints, it was undoubtedly our least considered option due to the difficulty of design and implementation. [2]

Decision-Making and Trade-Off

Referring to the design space exploration done in the previous section, we can derive a simple comparison in the following table.

As we have mentioned in our constraints, the goal of our overall system is to be low-powered, area-efficient, at a medium resolution (about 3-4 bits), and have a relatively fast throughput (about 10 MHz). When we evaluated our analog design experience as a team, we found that we may only be capable of relatively simple circuits with absolute success. For these reasons, we ruled out the SAR and TDC ADCs due to their complexity and inexperience with the design process. We then decided to focus on the Flash ADC despite its lackluster characteristics compared to the Pipelined ADC. This was mainly due to our unfamiliarity with the open-source tools needed to develop our circuit. Another reason was that we would have needed to create a Flash ADC to design a Pipelined ADC in the first place. Therefore, we concluded that first designing a Flash ADC would satisfy our design requirements at this stage of the development process.

ADC Architecture	Positives	Negatives
Flash	+ Highest throughput + Simplest design conceptually	- High input capacitance - Exponentially increasing power consumption and area requirement with system resolution
Pipelined	+ High throughput + Digital correction	- Require a clocked input - Latency between stages
SAR	+ Very accurate + Low power consumption and area requirement	- Slower throughput - Relatively challenging to implement
TDC	+ Incredibly energy and area-efficient + Immune from input signal noise + Can be implemented in a fully digital application	- Relatively slow throughput - Very difficult to implement - Implementation would require changing several other circuits

Table 7: ADC architecture comparisons

4.3 Proposed Design

Overview

Figure 5, shown below, is a general overview of the basic ReRAM crossbar that takes in a digital value at the DAC and returns a digital value from the ADC after running the computation through the crossbar.

Figure 5 shows a top-level block diagram of our design. A digital value will be input through the DAC, converting it to an analog value. These analog voltages run through the crossbar and the individual ReRAM cells creating a current. These currents are accumulated along the columns and collected by the corresponding TIA, which converts the current back into a voltage. This analog voltage is then run through the ADC, which converts it back into a digital voltage, allowing it to be read by a logic analyzer.

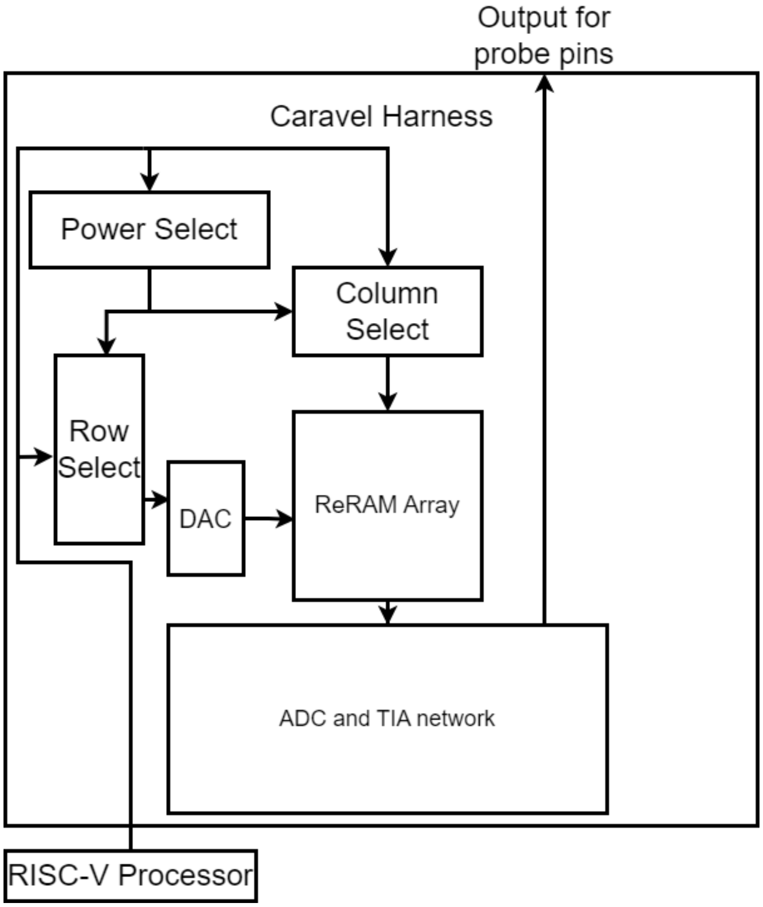


Figure 5: General Diagram for the overall design

Detailed Design and Visuals

An individual ReRAM cell is shown in Figure 7. Our crossbar will consist of an eight-by-eight array of these cells, as described previously in the overview. It can be seen that each cell contains both a resistor and a transistor, hence why this architecture is referred to as a 1T1R (one transistor one resistor) cell. The cell's Word Line (WL) will be connected to a logic analyzer that determines whether the cell should be on or off and powers it accordingly. The Bit line (BL) is connected to the DAC and is the voltage passed into the cell. The Source Line (SL) is where the current will accumulate and be output to the TIA.

We will use these cells to perform a MAC operation. This operation is illustrated in Figure 8, where the input voltages, V1, V2, and V3, are multiplied by the conductance's, G1, G2, and G3 of the ReRAM, and the resulting currents are then summed down along the column to create one output.

The conductance of a ReRAM cell depends on whether the cell is in an LRS(low resistance state) or an HRS(high resistance state). A LRS is viewed as a "digital 1" and a HRS as a "digital 0". All ReRAM cells start in a pristine state and must initially form into a LRS. After the initial form, the cell can be set and reset to switch between a digital 1 or 0. This process is illustrated in Figure 9.

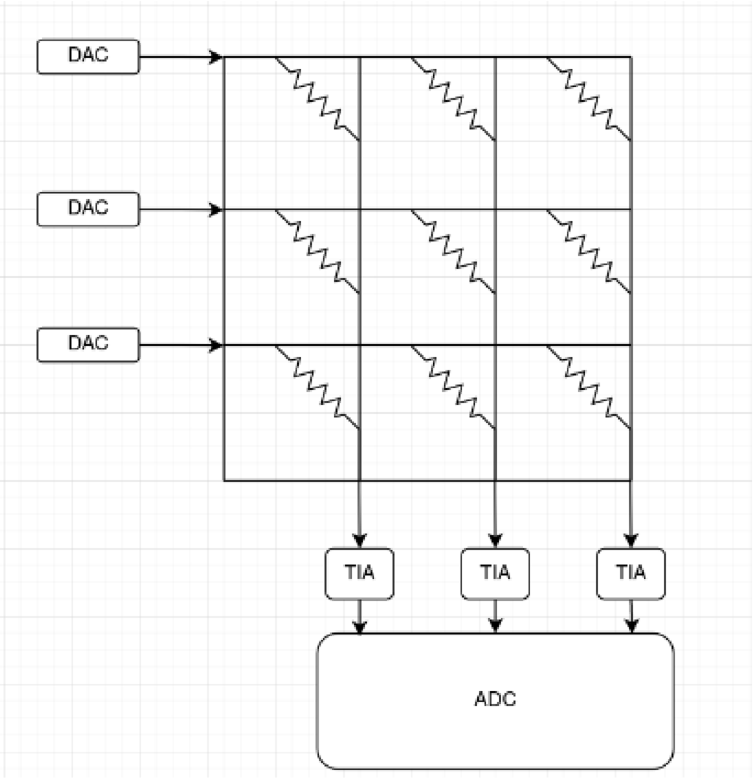


Figure 6: Diagram of crossbar configuration

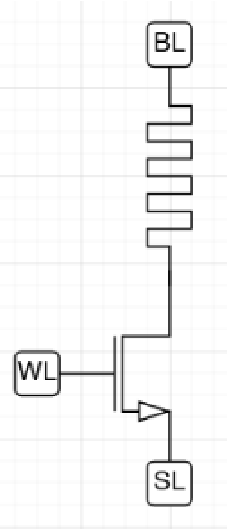


Figure 7: Diagram of 1T1R memristor

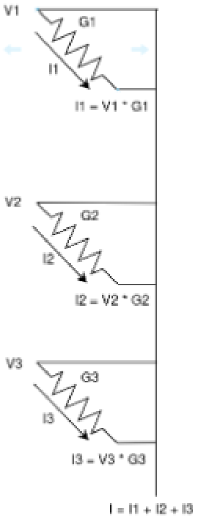


Figure 8: Example of vector-matrix computation

Functionality

Since this device is currently projected to be used in a research-oriented environment, the device should function appropriately. However, it does not need to have an expansive user interface. The device needs input-output pins clearly defined in the documentation and easily accessible. The pins should provide simple but valuable information, such as the values going into and out of the ADC and the DAC, TIA input and output, and possible output values of the individual memory cells or columns if the pin space is limited. This will allow professors, graduate, and undergraduate researchers to thoroughly understand how the device is functioning to verify correct operation.

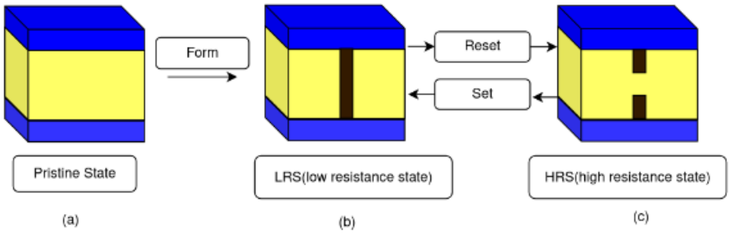


Figure 9: Illustration of memristor forming process

Areas of Concern and Development

The main concern of the project right now is fully designing our supporting analog devices and getting them to pass the LVS and DRC checks. There are many steps involved in these two checks, such as creating a design, schematic, and layout. These different steps must all match, so completing this for all of our analog circuits can be time-consuming. Another area of concern is the inaccurate spice models of the transistors in weak and moderate inversion and the memristors.

4.4 Technology Considerations

- Simulation tools:
  - ○ Ngspice
    - Easily integrates with schematic software
    - Cannot simulate Verilog-A
    - Easy to use
- Schematic and Layout tools:
  - ○ Xschem
    - Integrates well into the Efabless framework
    - Used for schematics
  - ○ Magic VLSI
    - Integrates well into the Efabless framework
    - Used for layout
  - ○ Cadence
    - It can be used for schematics and layout
    - It does not work with the technology/ process we are using
    - It could be used for creating proof-of-concept designs

4.5 Design Analysis

We are still in the process of implementing our design, so we cannot determine the functionality of our plan at this time. At this point, we have started designing our surrounding analog circuits, such as the ADC and TIA, and building the crossbar functionality. So far, there are no implications that the overall functionality of our circuit will not work. The plans for the circuits that we have currently may also change in the future as functionality requirements may change, and things might need to be added or removed.

5 Testing

5.1 Unit Testing

The following analog components are tested individually via Xschem, Ngspice, and GAW to ensure correct behaviors:

- 2:1 analog multiplexers
  - Tests will be done by introducing excitation signals equivalent to relative operational codes from the control module and power signals
  - Results are expected to follow the general 2:1 multiplexer output per the relative operational codes and power signals
- Memristor
  - Tests will be done by varying a voltage input to simulate the differing operating modes we have established (See Ideation)
  - At this stage of the project, expected outputs should clearly define specific currents that intuitively derive the differing operating modes
- Transistor switch
  - Tests will be done by simply performing a DC analysis to determine the switch impedance and drain current
  - Resulting switch impedances are expected to be as low as possible, and the drain current should be as high as possible
- 4-bit Flash ADC
  - Test will be done to identify the key ADC parameters
    - ENOB (Effective number of bits)
    - SNR (Signal to noise ratio)
    - INL (Integral nonlinearity)
    - DNL (Differential nonlinearity)
    - THD (Total Harmonic Distortion)
    - SFDR (Spurious Free Dynamic Range)
  - A triangle wave will be used at the input of the ADC
  - Spectral analysis will then be used to determine parameters
- Transimpedance (Voltage-to-Current) amplifier
  - Tests will be done by inputting an expected current based on previous DC analysis on the ReRAM crossbar and measuring the output voltage

  - Expected output voltages should indicate the differing input currents and provide a generous and intuitively quantized range of voltages for the ADC

- Strong arm comparator
  - Tests will be done by introducing a sine wave 5 to -5 Vpp and an ideal clock at 10 MHz to the circuit
  - Results should show that the comparator successfully switches between low and high output voltages when the input wave passes the threshold voltage of 3.3 V
- 1-bit DAC (Basic CMOS inverter)
  - Critical parameters to be established from this device are the behavioral performance in which a simple DC analysis should suffice.
  - Results should show that the 1-bit DAC correctly follows general inverter behavior.

The following digital components are to be tested individually via GTKwave to ensure correct behaviors:

- External FPGA control module
  - Tests will be done via a Verilog testbench that demonstrates all possible output operational codes
  - Expected results should follow the determined operational codes shown in
- Logic analyser
  - Fully digital device, so testing for this device will consist of thorough test benches for each input.
    - Most testing will be applicable once system integration occurs
    - testing before system integration is to test the functionality of the opcodes that we produce

- 3:8 Decoder
  - Tests will be done via a Verilog testbench that demonstrates an output sequence
  - Expected results should follow the general 3:8 decoder table
- 16:4 Priority encoder
  - Tests will be done via a Verilog testbench that demonstrates an output sequence
  - Expected results should follow the general 16:4 priority encoder table

Once the behaviors of each component have been determined, a layout will be realized in Magic VLSI. Layouts will be completed once DRC and LVS tests have been passed.

5.2 Interface Testing

As a whole, this project will consist of the following primary components, as stated in section 4.2: Logic analyzers, analog multiplexers, 3:8 decoders, 1-bit DACs, a ReRAM crossbar, TIAs, and 4-bit ADCs. Many of these components, specifically the 4-bit ADC and ReRAM crossbar, are built of several smaller components, there are several tests conducted to ensure the systems are operating as expected.

- **4-bit ADC:**
  As this project utilizes a 4-bit flash ADC, the following components are used: 16 comparators, a resistor ladder, and a 16:4 priority encoder. Once the ADC has been assembled, it is paramount that the encoding, integral nonlinearity (INL), and adequate number of bits (ENOB) are determined. A DC analysis will be conducted with a sweeping input voltage that simulates expected voltages based on the TIA output to test this.

5.3 Integration Testing

Integration testing in our project, aside from general component test benches, concerns the following critical junctions:

- **TIA to ADC:**
  This connection is vital to ensure correct ADC quantization regarding the TIA output range. In particular, this test will be done primarily in Xschem and Ngspice as both components are analog. The test will introduce the existing excitation signal referenced from the ReRAM crossbar during an individual test cited in section 5.1. The expected results should follow the relative output voltages established by the determined ADC encoding sequence.
- **Wrapper to overall system:**
  To pass the MPW precheck such that our project is valid for fabrication, we'll need to ensure that the input and output pins are correctly integrated. Specifically, the connections of interest are between the input power pins and the voltage level shifters and between the GPIO and logic analyzers. These connections can be tested through Xschem and Ngspice. The test plan should introduce an expected voltage through input pins based on listed pin behaviors and measure the corresponding outputs to ensure the correct voltages are delivered.

5.4 System Testing

The overall system tests will be performed primarily in Xschem and Magic VLSI. Firstly, the complete circuit behavior will be established using a similar test determined in section 5.3 for the wrapper to the overall system. Secondly, the final layout will be constructed using layouts of each primary component. Once the final layout passes DRC and LVS checks, it will be flattened, and a parasitic extraction (PEX) via Ngspice will be performed.

5.5 Regression Testing

We can cite the previous test results of our primary components to prevent new additions from breaking original functionality. This is plausible as the circuit was developed modularly, and input dependencies are clearly defined in section 4. Due to these defined expectations and influences, it should be possible to troubleshoot future functionality errors introduced by additional components quickly. However, it should still be noted that the following critical functions remain error-free or unchanged:

- ReRAM operations: The memristor operations determined by the established control voltages must be preserved, as doing otherwise will lead to cascading issues in control and interfacing circuits.
- Clock speed: Since the ADC comparators rely on the clock and have been sized accordingly, the clock speed should remain unchanged lest the pervasive effects of changing ADC characteristics can be accounted for.

5.6 Acceptance Testing

The functional results of this project can then be verified once all previous tests have been completed. These results can be illustrated and condensed via measurements from the Xschem, as mentioned earlier, analysis to confirm behavioral design constraints have been satisfied. Next, DRC and LVS report logs can easily demonstrate the overall success of component and project integration. Finally, fabrication constraint satisfaction can be illustrated through post-layout simulations like PEX and the MPW precheck. It should also be noted that systemic noise is another concern that must be addressed. This parameter can be tested by measuring and calculating the SNR of the system in its entirety or through the individual test benches indicated in the Results section.

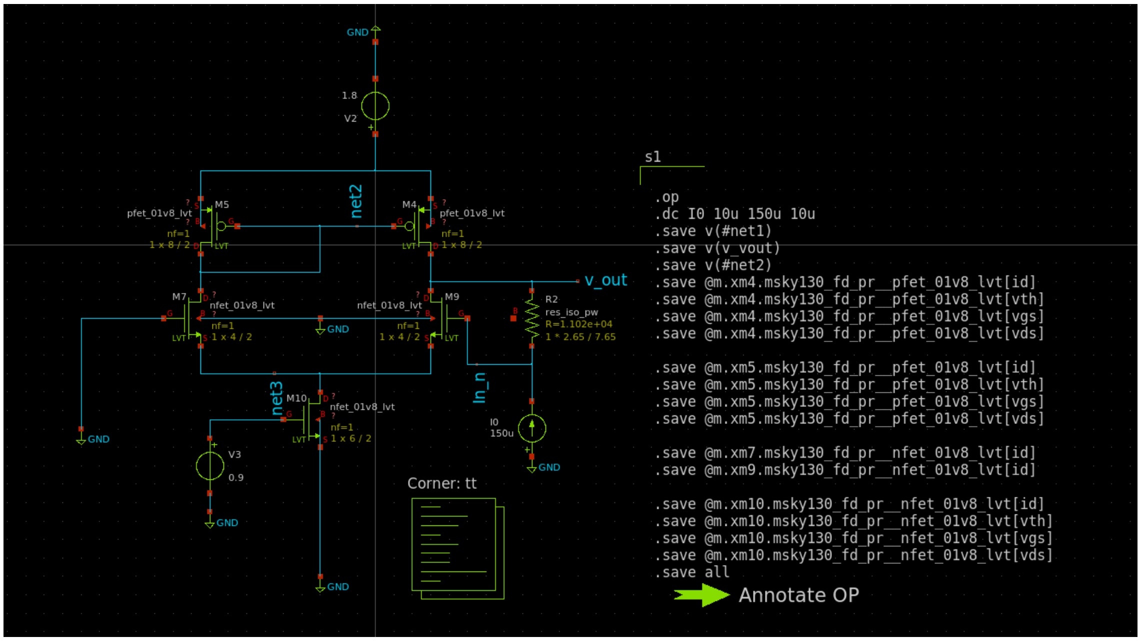
5.7 Results

As described in the previous sections, modular tests for analog components will be conducted in Xschem. These test benches are illustrated in Figures 10 through 12.

6 Implementation

We have created a design plan or have designed most of the individual components for our design. We have also begun to push individual components through our tool flow and, as of now, have been able to go through our 1-bit DAC.

Next semester, we plan to finalize the layouts and testing of the individual components, create layouts that pass LVS, and verify their functionality. After we have validated our components, we plan to integrate them into the Caravel harness, where we will run numerous simulations to test functionality and fix any issues we run into while doing so. This must be completed by November so we can submit our design to the Efabless shuttle program for fabrication.



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.dc I0 10u 150u 10u
.save v(#net1)
.save v(v_vout)
.save v(#net2)
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.save @m.xm9.msky130_fd_pr__nfet_01v8_lvt[id]

.save @m.xm10.msky130_fd_pr__nfet_01v8_lvt[id]
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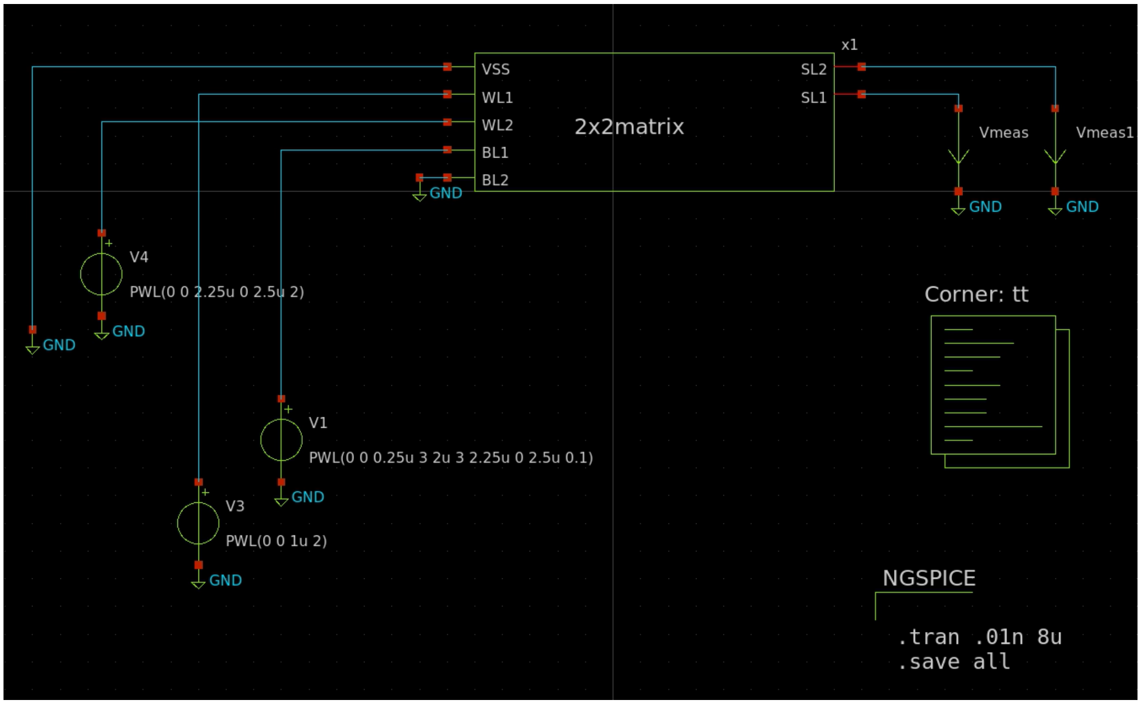
.save @m.xm10.msky130_fd_pr__nfet_01v8_lvt[vgs]
.save @m.xm10.msky130_fd_pr__nfet_01v8_lvt[vds]
.save all
```

Figure 10: Testbench for TIA



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.save all
```
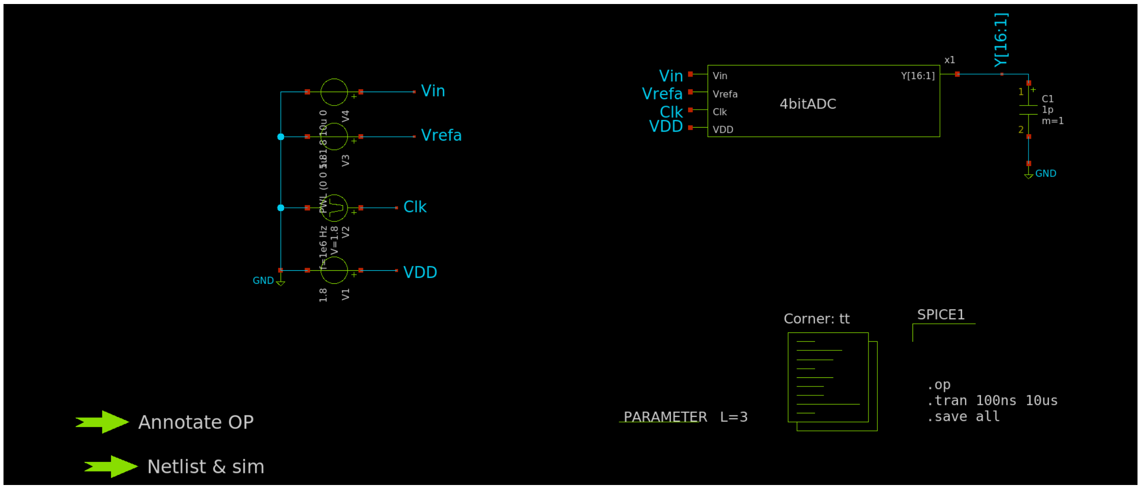

Figure 11: Testbench for 2x2 ReRAM crossbar



```
.op
.tran 100ns 10us
.save all
```

Figure 12: Testbench for ADC resistor/comparator ladder

7 Professional Responsibility

7.1 Areas of Responsibility

7.2 Project Specific Professional Responsibility Areas

- **Work Competence**
  This responsibility is essential for our project. Our project is particular, so the design of components needs to be well thought out and of high quality. We must also stay on task for our design as we have a strict deadline of when the project must be submitted for fabrication. We are doing an excellent job at ensuring we are progressing, and barring any unforeseen circumstances, we should be able to meet the deadline.

- **Financial Responsibility**
  This is not an applicable responsibility as everything we do is through open-source tools and, therefore, free. The only cost that we will have is time.

- **Communication Honesty**
  This applies to our design as our project is open source, and to have the chance to have it fabricated, we will need to submit our design to the open-source documentation. This means we will need good documentation and clarity of our design so that when other people look at it, they might understand what it is for. We must also be transparent when discussing our design with our advisor and avoid lying about what progress we have made. We have been doing an excellent job with this and communicating effectively and clearly with our clients.

- **Health,Safety, and Well-being**
  This product will not be able to cause any potential health risks to the users and, therefore, has no impact on our design.

- **Property Ownership**
  All property we will be using is open source and free for anyone to use. However, we will still respect the work of those who have gone before us.

- **Sustainability**
  Not a relevant responsibility, chip fabrication can be harmful to the environment. However, we

are not in charge of the manufacturing process and, therefore, do not affect the conservation of resources.

- **Social Responsibility**
  Our product can potentially improve computational technology by creating a device that can do computation with less chip area and lower power consumption.

Area	Description	NSPE Canon	IEEE Code of Ethics
Work competence	Perform work of high quality, integrity, timeliness, and professional competence	Perform services only in areas of their competence; Avoid deceptive acts.	5. to improve the understanding of technology, its appropriate application, and potential consequences 6. to maintain and improve our technical competence and to undertake technological tasks for others only if qualified by training or experience or after full disclosure of pertinent limitations
Communication Honesty	Report work truthfully, without deception, and is understandable to stakeholders	issue public statements objectively and truthfully. Avoid deceptive acts.	3. to be honest and realistic in stating claims or estimates based on available Data; 2. to avoid real or perceived conflicts of interest whenever possible and to disclose them to affected parties when they do exist
Health, safety, and well-being	Minimize risks to safety, health, and well-being of stakeholders	Hold paramount the public's safety, health, and welfare.	1. to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment 9. to avoid injuring others, their property, reputation, or employment by false or malicious action

Financial responsibility	Deliver products and services of realizable value and at reasonable costs	Act for each employer or client as faithful agents or trustees	4. to reject bribery in all its forms
Property ownership	Respect property, ideas, and information of clients and others	Act for each employer or client as faithful agents or trustees.	9. to avoid injuring others, their property, reputation, or employment by false or malicious action
Sustainability	Protect the environment and natural resources locally and globally		1. to accept responsibility in making decisions consistent with the safety, health, and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;
Social Responsibility	Produce products and services that benefit society and communities	Conduct themselves honorably, responsibly, ethically, and lawfully to enhance the profession's honor, reputation, and usefulness.	8. to treat fairly all persons and to not engage in acts of discrimination based on race, religion, gender, disability, age, national origin, sexual orientation, gender identity, or gender expression 9. to avoid injuring others, their property, reputation, or employment by false or malicious action 10. to assist colleagues and co-workers in their professional development and to support them in following this code of ethics.

Table 8: Areas of responsibility

7.3 Most Applicable Professional Responsibility Area

The most applicable responsibility to our project is Work Competence. This is because ASIC design is a very intensive process that requires a lot of intricate details and thought processes. The scale of the project is also quite large, and to meet our goals, we must ensure that we are staying on task and making high-quality progress. Our design will be added to the open-source documentation when we are finished, so we must create high quality work so that others may use it as inspiration.

8 Closing Material

8.1 Discussion

While this project is still a work in progress, we expect to have a fully functional ReRAM crossbar working by the end of the class. This ReRAM crossbar will be able to have values written to individual cells, and then when a voltage is applied, it will perform a compute. We have verified that the individual components will work as intended. Now, we need to integrate them to test the circuit as a whole. This will be achievable with time and effort.

8.2 Conclusion

We have completed our research for this design and are currently working on implementing and testing the surrounding analog circuits that we will need. We have pushed the one but DAC through our toolflow and are currently working on the ADC and the TIA. We have also started working on simulating the crossbar and implementing a logic analyzer. By the end of this project, we hope to integrate these components to form a working crossbar. The biggest constraint that we have had so far is a lack of time to work on these subcircuits.

8.3 References

[1] T. C. Carusone, K. W. Martin, and D. Johns, Analog Integrated Circuit Design, 2nd Edition, 2nd ed. Hoboken, NJ: John Wiley & Sons, 2011.

[2] W. Li, P. Xu, Y. Zhao, H. Li, Y. Xie and Y. Lin, "Timely: Pushing Data Movements And Interfaces In Pim Accelerators Towards Local And In Time Domain," 2020 ACM/IEEE 47th Annual International Symposium on Computer Architecture (ISCA), Valencia, Spain, 2020, pp. 832-845, doi: 10.1109/ISCA45697.2020.00073.

[3] "Sky130_fd_pr_reram - sky130 reram (Skywater provided)¶," sky130_fd_pr_reram - SKY130 ReRAM (SkyWater Provided) - SkyWater SKY130 PDK 0.0.0-22-g72df095 documentation, https://sky130-fd-pr-reram.readthedocs.io/en/latest/index.html (accessed Apr. 14, 2024).

[4] C. Xu et al., "Overcoming the challenges of crossbar resistive memory architectures," 2015 IEEE 21st International Symposium on High-Performance Computer Architecture (HPCA), Burlingame, CA, USA, 2015, pp. 476-488, doi: 10.1109/HPCA.2015.7056056. keywords: Arrays;Random access memory;Phase change materials;Switches;Resistance;Transistors.

[5] IEEE Standards Association, https://standards.ieee.org/ (accessed Apr. 23, 2024).

8.4 Appendices

Manuals:

- **Magic Docs:** http://opencircuitdesign.com/magic/index.html
- **Netgen Docs:** http://opencircuitdesign.com/netgen/index.html
- **Xschem Docs:** https://xschem.sourceforge.io/stefan/xschem_man/xschem_man.pdf
- **Ngspice Docs:** https://ngspice.sourceforge.io/docs/ngspice-40-manual.pdf

9 Team

9.1 Team Members

- Electrical Engineers
  - Konnor Kivimagi
  - Gage Moorman
  - Jason Xie
- Computer Engineers
  - Nathan Cook

9.2 Required Skill Sets

- Analog design
  - Layout design
  - Schematic design
  - Basic circuit knowledge
  - Device sizing
- Digital design
  - Verilog
  - Knowledge of computer architecture

9.3 Skill Sets

Skill	Members
Layout Design	All members
Schematic design	All Members
Basic circuit knowledge	All Members
Device sizing	Gage Moorman Jason Xie
Verilog	All Members
Knowledge of computer architecture	Nathan Cook, Jason Xie

Table 9: Required Skills

9.4 Project Management Style

Our project management style was agile. We divided our time into short one-week sprints where, after each week, we discuss and document our progress and address any outstanding issues and concerns.

9.5 Initial Project Management Roles

- Gage Moorman - Team Organizer, main analog designer
- Konnor Kivimagi - Main documentation editor, mixed analog, digital designer
- Nathan Cook – Main client liaison, mixed analog, digital designer
- Jason Xie – Assistant documentation editor, main digital designer

9.6 Team Contract

Team Members:

1. Gage Moorman
2. Nathan Cook
3. Konnor Kivimagi
4. Jason Xie

Team Procedures:

1. Day, time, and location (face-to-face or virtual) for regular team meetings:
   Ideally, on Friday evenings, in person, Coover TLA and Durham 310 lab.

2. Preferred method of communication updates, reminders, issues, and scheduling (e.g., email, phone, app, face-to-face):
   Email, Microsoft Teams, Face-to-face, and or Discord will be used to coordinate with other group members, ideally Microsoft Teams, so that we can keep all group information in one place.

3. Decision-making policy (e.g., consensus, majority vote):
   A consensus will make decisions.

4. Procedures for record keeping (i.e., who will keep meeting minutes, how will minutes be shared or archived):
   Start a Microsoft Teams meeting, keep notes in Microsoft Teams as the meeting progresses, and assign Gitlab tasks. Use GitLab to chronicle work done.

Participation Expectations

1. Expected individual attendance, punctuality, and participation at all team meetings:
   Ideally, attend all meetings on time, but if absences occur, the members should notify the group of the absence; the rest will document what was discussed and send absentee the meeting notes.

2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines:
   Each member should try to complete their assignments and reach their deadlines within the ideal time commitment (8 hours) each week; if not met, it is not automatically an issue unless it becomes a recurring problem.

3. Expected level of communication with other team members:
   Responses should be timely; a few hours are okay, but at least a response within the day would be ideal.

4. Expected level of commitment to team decisions and tasks:
   Should be available and willing to meet on weekends to finish tasks or work later, ideal time commitment is 8 hours a week.

Leadership

1. Leadership roles for each team member (e.g., team organization, client interaction, individual component design, testing, etc.):
   may be changed as deliverables are updated throughout the project run. The client and advisor gave baseline deliverables; if those are met, other deliverables will be given.

   - Nathan Cook: Main client liaison, mixed analog, digital designer
   - Gage Moorman: Team Organizer, main analog designer

- Jason Xie: assistant documentation editor, main digital designer
- Konnor Kivimagi: Main documentation editor, mixed analog, digital designer

2. Strategies for supporting and guiding the work of all team members:
   Agile project management, using GitLab to assign tasks, filling meeting notes with relevant information on tasks that must be completed.

3. Strategies for recognizing the contributions of all team members:
   Weekly reporting during agile meetings and Gitlab push and issue resolution.

Collaboration and Inclusion

1. Describe each team member's skills, expertise, and unique perspectives.
   - Nathan Cook: Computer Architecture, semiconductor physics, Computer science
   - Gage Moorman: Signals processing, Digital Synthesis
   - Jason Xie: Computer Architecture, Microwave, and RF, Digital Synthesis
   - Konnor Kivimagi: Signals processing, Semiconductor physics

2. Strategies for encouraging and supporting contributions and ideas from all team members:
   Agile project management to issue ideas as well as troubles with deliverables as well as GitLab issue reviews when deliverables or portions of work are finished.

3. Procedures for identifying and resolving collaboration or inclusion issues (e.g., how will a team member inform the team that the team environment is obstructing their opportunity or ability to contribute?)
   Inform the person one on 1 to try and resolve the issue. If no resolution is found, move to a group setting, which might involve the client and advisor if it is a project-related issue that further questions can resolve; the last resort is going to 491 TAs or Professors to see what can be done to resolve it.

Goal-Setting, Planning, and Execution

1. Team goals for this semester:
   Finishing all deliverables expected for this semester between the group, client, and advisor and being ready for or already working on deliverables for the fall.
   - Current deliverables
     - Familiarise ourselves with project tools (Caravel, GTKwave, Klayout, magic, XScheme)
     - Begin basic work on designs, laying circuits out on paper and then converting them over to the tools
   - Future deliverables
     - Improve upon previous groups' work
     - Better resolution ADC
     - Fix ReRAM LVS
     - Bit serial computation DAC

2. Strategies for planning and assigning individual and teamwork:
   Meeting on Fridays to set group and individual tasks for the next week and go over work done during the week to see if there is any place lacking and if that place needs extra support from other group members

3. Strategies for keeping on task:
   Regularly checking in with the group and their progress, giving gentle reminders, using gitlab to keep track of work on the project and who is doing what issues and which ones are getting resolved.

Consequences for Not Adhering to Team Contract

1. How will you handle infractions of any of the obligations of this team contract?
   Three strike system, 1st will be a gentle reminder, 2nd will be a group conversation about what needs to change 3rd refer to continued infractions

2. What will your team do if the infractions continue?
   Consult 491 professors about what we should do and continue to dialogue with the group and the professors.

****

a) *I participated in formulating this contract's standards, roles, and procedures.*

b) *I understand that I must abide by these terms and conditions.*

c) *I understand that if I do not abide by these terms and conditions, I will suffer the consequences as stated in this contract*

Nathan Cook	DATE 1/26/2024
Gage Moorman	DATE 1/26/2024
Konnor Kivimagi	DATE 1/26/2024
Jason Xie	DATE 1/26/2024

Abbreviations Glossary

ADC - Analog to Digital Converter

ASIC - Application Specific Integrated Circuit

DAC - Digital to Analog Converter

DRC - Design Rule Check

LVS - Layout Vs Schematic

ReRAM - Resistive Random Access Memory

TDC - Time to Digital Converter

TIA - Transimpedance Amplifier (Current to Voltage Amplifier)

(add alphabetically)